WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a first interconnection which is made of materials containing copper as a principal ingredient and has a given width, length, thickness and volume;

a second interconnection which is made of materials containing copper as a principal ingredient and provided above said first interconnection; and

at least one via contact which is made of materials containing copper as a principal ingredient and through which said first interconnection and said second interconnection are electrically connected to each other, said at least one via contact including one via contact which is provided when one of the width and the volume of said first interconnection is not larger than a given value and a plurality of via contacts, which are arranged at regular intervals, each of which is not larger than a given value, in a predetermined region of said first interconnection, when one of the width and the volume of said first interconnection exceeds a given value.

2. The semiconductor integrated circuit device according to claim 1, wherein voids are unevenly centralized in a contact position of said first interconnection to which said at least one via contact is connected.

3. The semiconductor integrated circuit device according to claim 1, wherein said one via contact is provided when the width and the length of said first interconnection are each 2 μm or less, and has a diameter of 0.2 μm or smaller.

4. The semiconductor integrated circuit device according to claim 1, wherein said plurality of via contacts are provided when the width and the length of said first interconnection each exceed 2 μm, and each have a diameter of 0.2 μm or smaller.

5. The semiconductor integrated circuit device according to claim 1, further comprising a third interconnection which is made of materials containing copper as a principal ingredient and formed in contact with one end of said first interconnection in a direction of the length of said first interconnection such that the third interconnection is flush with the first interconnection, the third interconnection having a given width, length, thickness and volume,

wherein said one via contact is provided when one of the width and the volume of said third interconnection is not larger than a given value.

6. The semiconductor integrated circuit device according to claim 5, wherein the width and the length of said third interconnection are each 2 μm or less and said one via contact has a diameter that is not larger than 0.2 μm.

7. The semiconductor integrated circuit device according to claim 1, further comprising a third interconnection which is made of materials containing copper as a principal ingredient and formed in contact with one end of said first interconnection in a direction of the length of said first interconnection such that the third interconnection is flush with the first interconnection, the third interconnection having a given width, length, thickness and volume,

wherein said plurality of via contacts are arranged at regular intervals, each of which is not smaller than a given value, in a predetermined region of said first interconnection when one of the width and the volume of said third interconnection exceeds a given value.

8. The semiconductor integrated circuit device according to claim 7, wherein the width and the length of said third interconnection each exceed 2 μm and said plurality of via contacts each have a diameter that is not larger than 0.2 μm.

9. The semiconductor integrated circuit device according to claim 1, wherein the predetermined region of said first interconnection is a void effective diffusion region in which voids included in said first interconnection are centralized by diffusion on a bottom of said via contact to cause a contact failure in said via contact.

10. The semiconductor integrated circuit device according to claim 9, wherein said void effective diffusion region is defined by an almost circular region at a radius of R from a center of the bottom of one of said plurality of via contacts in which the largest number of voids are centralized.

11. The semiconductor integrated circuit device according to claim 10, wherein the radius R is given by $R = (F \cdot t)^{0.5}$ where F is a diffusion coefficient and t is diffusion time.

12. The semiconductor integrated circuit device according to claim 10, wherein the radius R is 25 μm.